HIGH-FREQUENCY POWER AMPLIFIER HAVING DIFFERENTIAL INPUTS

BACKGROUND OF THE INVENTION

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1. FIELD OF THE INVENTION

The present invention relates to a high-frequency power amplifier having differential inputs, and more specifically to a high-frequency power amplifier having differential inputs, capable of simplifying a structure of an

10   output port of a communication system for 2.4 GHz ISM frequency band by designing and producing a high-frequency power amplifier having differential inputs for 2.4 GHz ISM frequency band using a silicon germanium (SiGe) microwave monolithic integrated circuit (MMIC).

2. BACKGROUND OF THE INVENTION

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Fig. 1 is a constructional view showing an output port of a conventional communication system.

As shown in Fig. 1, a high-frequency transmission unit 10 of a conventional communication system has two output terminals. The signals

20   output from the two output terminals are have phases inverted each other, and this output is referred to as "a balance output".

On the other hand, a conventional power amplifier 30 for amplifying and sending a signal to an antenna 40 has one input terminal and one output terminal. Therefore, a signal, which can be received by the conventional

25   power amplifier 30, is so called "an unbalance signal". The unbalance

signal means a signal not having a phase inverted from other signals.

Therefore, in order to amplify the signals output from a high-frequency transmission unit and send the amplified signals to the antenna, a signal conversion unit 20 for converting the balance signal into the unbalance signal and sending the unbalanced signal to an output amplifier is required. Generally, a balanced-to-unbalanced element (e.g. a BALUN element) which is a passive element is used as the signal conversion unit 20.

Accordingly, in the conventional power amplifier 30, there is a problem that the input signal is attenuated due to a characteristic of the BALUN element used in signal conversion.

Therefore, in the conventional power amplifier 30, the signal attenuated due to the BALUN element must be compensated to satisfy an output power of the antenna 40 required for the communication system. In other word, there is a problem that a power gain required for the power amplifier is increased.

SUMMARY OF THE INVENTION

The present invention is contrived to solve the above problems, and thus it is an object of the present invention to provide a high-frequency power amplifier having differential inputs, capable of obtaining an output power of an antenna required for a communication system without any attenuation by implementing an active element of a silicon germanium (SiGe) microwave monolithic integrated circuit (MMIC) as a conversion element for converting a balance signal into an unbalance signal.

Furthermore, it is another object of the present invention to provide a

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high-frequency power amplifier having differential inputs, having functions of breaking and controlling a power implemented in an output port of a communication system as well as a function of amplifying an output signal of a high-frequency transmission unit and sending the amplified signal to an antenna by using a silicon germanium (SiGe) microwave monolithic integrated circuit (MMIC).

Furthermore, it is still another object of the present invention to provide a high-frequency power amplifier having differential inputs, capable of reducing the number of elements in a transmission unit of a communication system and a cost for the communication system by simplifying a structure of an output port of the communication system for 2.4GHz ISM frequency band.

In order to achieve the above objects, a high-frequency power amplifier having differential inputs according to the present invention comprises: a power supply unit; a first amplification circuit unit for amplifying high-frequency differential input signals of differential input terminals INA, INB into outputting a single high-frequency signal; an intermediate impedance matching unit for impedance-matching the single high-frequency signal amplified by the first amplification circuit unit; a second amplification circuit unit for receiving and amplifying the impedance-matched single high-frequency signal from the intermediate impedance matching unit and outputting the amplified signal to an antenna through an output terminal thereof; a power control circuit unit for controlling a power output to the antenna through the output terminal of the second amplification circuit unit by varying a voltage of a power control

terminal; a first bias circuit unit for determining an operation reference point of the first amplification circuit unit; and a second bias circuit unit for determining an operation reference point of the second amplification circuit unit.

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BRIEF DESCRIPTION OF THE DRAWINS

The above and other objects, advantages and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in

10   which:

Fig. 1 is a constructional view showing an output port of a conventional communication system,

Fig. 2 is a constructional view showing functional units of a conventional high-frequency power amplifier,

15   Fig. 3 is a constructional view showing an output port of a communication system using a high-frequency power amplifier having differential inputs according to the present invention,

Fig. 4 is a constructional view showing functional units of a high-frequency power amplifier having differential inputs according to the

20   present invention, and

Fig. 5 is a circuit diagram showing a high-frequency power amplifier having differential inputs according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25   Now, preferred embodiments of the present invention will be

described in detail with reference to the accompanying drawings.

Fig. 3 is a constructional view showing an output port of a communication system using a high-frequency power amplifier 31 having differential inputs according to the present invention.

5   As shown in Fig. 3, the output port of the communication system according to the present invention includes a high-frequency transmission unit 10 and a high-frequency power amplifier having differential inputs 31. Two output signals OUTA, OUTB output from the high-frequency transmission unit 10 are input to the high-frequency power amplifier 31 having differential inputs, and the high-frequency power amplifier 31

10   outputs a single output signal amplified using a voltage difference between the two signals OUTA, OUTB to an antenna.

Fig. 4 is a constructional view showing functional units of a high-frequency power amplifier having differential inputs according to the present invention. As shown in Fig. 4, the high-frequency power amplifier

15   present invention. As shown in Fig. 4, the high-frequency power amplifier having differential inputs includes a first amplification circuit unit 60, a second amplification circuit unit 80, an intermediate impedance matching unit 50, and a bias/control block 70.

The first amplification circuit unit 60 has difference inputs to

20   perform a function as a signal conversion unit 20, and the second amplification circuit unit 80 is a common emitter power amplifier of class AB.

The intermediate impedance matching unit 50 matches an output impedance of the first amplification circuit unit 60 and an input impedance

25   of the second amplification circuit unit 80 to minimize a reflection loss of a

high-frequency signal, thereby to maximize a power of the high-frequency signal input to the second amplification circuit unit 80.

The bias/control block 70 includes bias circuit units of the first amplification circuit unit 60 and the second amplification circuit unit 80, a power breaking circuit unit, a power controlling circuit unit.

Now, a construction of a high-frequency power amplifier having differential inputs according to the present invention will be described in detail with reference to Fig. 5.

As shown in Fig. 5, the first amplification circuit unit 60 includes a seventh transistor Q7, an eighth transistor Q8, a first inductor L1, and differential input terminals INA, INB. The first inductor L1 serves as a negative feedback circuit for stabilizing the first amplification circuit unit 60.

The second amplification unit 80 is a class AB common emitter power amplifier including a twelfth transistor Q12 and a fifth capacitor C5.

The intermediate impedance matching unit 50 includes a third capacitor C3, a second capacitor C2, and a sixteenth resistor R16.

The bias/control block 70 includes the bias circuit unit of the first amplification circuit 60, the bias circuit unit of the second amplification unit 80, a power breaking circuit unit, and a power controlling circuit unit.

The bias circuit unit of the first amplification circuit unit 60 includes a fifth transistor Q5, a sixth transistor Q6, a plurality of resistors R11~R15 and a first capacitor C1. The bias circuit unit of the first amplification circuit unit 60 comprises a bias current mirror circuit for compensating for variation in a current gain of the first amplification circuit unit. The bias

circuit unit of the first amplification circuit unit 60 serves for determining an operation reference point of the first amplification circuit unit 60.

The bias circuit unit of the second amplification circuit unit 80 includes a tenth transistor Q10, an eleventh transistor Q11, a plurality of resistor R18~R20 and a forth capacitor C4. The bias circuit unit of the second amplification circuit unit 80 comprises a bias current mirror circuit for compensating for variation in a current gain of the second amplification circuit unit. The bias circuit unit of the second amplification circuit unit 80 serves for determining an operation reference point of the second amplification circuit unit 80.

The resistors R11, R13~R15, R18~R20 and the first and forth capacitors C1, C4 are elements for stabilizing base voltages of the transistors.

The power breaking circuit unit includes a plurality of resistors R23~R25, voltage-controlled current sources SRC1, SRC2 and a fifth transistor Q15.

The power controlling circuit unit includes a plurality of resistors R1~R5, R10, R17, and a plurality of capacitors Q1~Q4, Q9, Q17. The seventh transistor Q17 serves as a protection diode for protecting inner circuits of the high-frequency power amplifier by absorbing a static electricity supplied to the power controlling terminal VCTRL 73.

Operations of the high-frequency power amplifier having differential inputs according to the present invention will be described in detail.

First, in the first amplification circuit unit 60, a voltage difference between two input signals input to two differential input terminals INA, INB

is amplified, and the amplified voltage difference is output to the intermediate impedance matching unit 50 in the form of a single signal from a collector of the eighth transistor Q8.

The intermediate impedance matching unit 50 matches an output impedance of the eighth transistor Q8 and an input impedance of the twelfth transistor Q12 using the third capacitor C3 which is an intermediate impedance matching element to output the single signal output from the eighth transistor Q8 to a base of the twelfth transistor Q12.

Therefore, a reflection loss of the single high-frequency signal output from the eighth transistor Q8 is minimized, whereby the power of the signal input to the twelfth transistor Q12 is maximized.

In the second amplification circuit unit 80, the twelfth transistor Q12 receives and amplifies the output signal of the eighth transistor Q8 matched with the third capacitor C3 which is an intermediate impedance matching element, and outputs the amplified high-frequency signal to an antenna 40 through an output terminal Vcc2_OUT of the second amplification circuit unit. The fifth capacitor C5 is an element for reducing an output high-frequency component of the second amplification circuit unit.

On the other hand, amplification factors of the first amplification circuit unit 60 and the second amplification circuit unit 80 are determined by bias currents supplied to collectors of the seventh, eighth and twelfth transistors, and procedures of supplying the bias current are as follows.

First, when a supply voltage Vcc is supplied to a supply voltage terminal VCC0 71 and a voltage which is the same as the supply voltage Vcc is supplied to the power control terminal VCTRL 73, the bias states of

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the circuits are as follows.

If a base current of the second transistor Q2 is ignored, a collector current of the first transistor Q1 is the same as a current L_c1 supplied to a forth resistor R4 as shown in Equation 1 as follows:

5 [Equation 1]

$$I\_c1 \fallingdotseq (V_{B1}-V_{BEONQ1})/R3$$

where a collector-emitter saturation voltage is ignored, V_{B1} is a base voltage of the first transistor Q1, and V_{BEONQ1} is a base-emitter turn-on voltage of the first transistor Q1.

10 A base voltage V_{B1} of the first transistor is determined by distributing a voltage V_{CTRL} of the power controlling terminal VCTRL 73 using a first resistor R1 and a second resistor R2 as follows:

[Equation 2]

$$V_{B1} \fallingdotseq V_{CTRL} \cdot (R2 / R1+R2).$$

15 When the first transistor Q1 is saturated, the collector voltage of the first transistor Q1 is the same as the emitter voltage thereof as follows:

[Equation 3]

$$V_{C1} \fallingdotseq I\_c1 \cdot R3.$$

A voltage V1 is a node voltage distributed by a fourth resistor R4

20 and a twelfth resistor R12 as follows:

[Equation 4]

$$V1 = V_{C1}+I\_c1 \cdot R4 = I\_{12} \cdot R12 + 2 \cdot V_{BEON}.$$

On the other hand, a reference current I_c2 of the third transistor is as follows:

25 [Equation 5]

$I\_c2 \fallingdotseq \{(R5+R7) \cdot V_{C1} - V_{BEONQ3} \cdot R5\} / (R5+R7).$

In other word, the reference current I_c2 of the third transistor is obtained by employing the voltage Vc1 obtained in the Equation 3 in the equation 5.

5   A collector current I_c3 of the fourth transistor is determined by the reference current L_c2 and emitter resistance ratio of the third transistor Q3 due to a current mirror relationship between the third transistor Q3 and the fourth transistor Q4 as follows:

[Equation 6]

10    $I\_c3 \fallingdotseq I\_c2 \cdot (R5/R10).$

In addition, assuming that the current I_12 is sufficiently lager than the current I_c1 and the current I_c3, the current I_12 is the same as the current I_ref as follows:

[Equation 7]

15    $I\_12 \fallingdotseq I\_ref \fallingdotseq \{Vcc-(2 \cdot V_{BEON})\} / (R26+R12)$

$\fallingdotseq \{Vcc-(2 \cdot V_{BEON})\} / (R22+R21)$

$\fallingdotseq \{Vcc-(Vc1+I\_c1 \cdot R4)\} / R26.$

In addition, a fifth transistor Q5, a seventh transistor Q7 and an eighth transistor Q8 of the first amplification circuit unit 60 form a current

20   mirror relationship, and a reference current of the current mirror is a current I_12.

In other word, bias currents I_1b, I_1a of the seventh transistor Q7 and the eighth transistor Q8 in the first amplification circuit unit are determined based on a ratio of the current I_12 : the current I_1b : the

25   current I_1a = 1 : 6 : 6 in accordance with on an area ratio of the transistor.

The bias current I_1b, I_1a is supplied from the supply voltage terminals VCC1A, VCC1B of the first amplification circuit unit. A voltage of the supply voltage terminal VCC1A, VCC1B of the first amplification circuit unit is the same as a supply voltage Vcc of the supply voltage terminal VCCO 71.

In addition, a collector current I_c4 of the ninth transistor Q9 is determined by the reference current I_c2 and emitter resistance ratio of the third transistor Q3 due to a current mirror relationship between the third transistor Q3 and the ninth transistor Q9 as follows:

[Equation 8]

$I\_c4 \fallingdotseq I\_c2 \cdot (R5/R17)$.

In the equation 7, assuming that the current I_ref is sufficiently lager than the current I_c4, a reference current in the current mirror relationship between the tenth transistor Q10 and the twelfth transistor Q12 can be a current I_ref.

In other word, a bias current I_2 of the twelfth transistor Q12 in the second amplification circuit unit 80 is determined based on a ratio of the current I_ref : the current I_2 = 1 : 16 in accordance with an area ratio of the transistor.

The current I_2 is supplied from the supply voltage terminal Vcc2_OUT. A voltage of the supply voltage terminal Vcc2_OUT in the second amplification circuit unit is the same as a supply voltage Vcc of the supply voltage terminal VCCO 71.

Accordingly, the bias currents I_1b, I_1a, I_2 determined by the procedures become the collector currents of the seventh transistor, the

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eighth transistor, and the twelfth transistor to determine signal amplification factors of the first amplification circuit unit and the second amplification circuit unit.

On the other hand, when producing an integrated circuit, the sixth transistor Q6 and the eleventh transistor Q11 compensate a change of a bias current due to a change rate of an current amplification factor of the transistor to safely maintain the bias current I_1b, I_1a, I_2.

In addition, the resistors R6~R9 stabilize base voltages of the fourth transistor Q4, the third transistor Q3, and the ninth transistor Q9.

On the other hand, procedures of controlling the power by the power controlling circuit unit are as follows.

In the operation of the power controlling circuit unit, the voltage of the power controlling terminal VCTRL 73 is controlled within a range of 0~Vcc [V] and bias currents of the first amplification circuit unit 60 and the second amplification circuit unit 80 are controlled, thereby controlling an output power of an antenna which is logarithmically proportional to the bias currents.   Procedures of the operation will be described as follows below.

First, according to Equation 1 and Equation 2, a base voltage V_{B1} of the first transistor Q1 and a bias current I_c1 of the first transistor Q1 are decreased.   Therefore, a base current of the second transistor Q2 can not be ignored.

Therefore, in a case of not including the first transistor Q1, a collector voltage V_{C1} of the first trnasister Q1 is determined as follows:

[Equation 9]

$$V_{C1} \fallingdotseq V1 - R_{L1} \cdot I\_c1$$

where the voltage 1 is a node voltage distributed by a fourth resistor R4 and a twelfth resistor R12 as shown in the equation 4. R_{L1} is an equivalent load resistor of the first transistor.

In other word, when a voltage of the power controlling terminal VCTRL 73 is decreased from the supply voltage to a ground voltage and the current I_c1 is decreased as shown in the equation 1, the collector voltage V_{C1} of the first transistor Q1 is increased as shown in the equation 9 and the collector current I_c2 of the third transistor Q3 as shown in the equation 5. Therefore, the current I_c3 is increased due to the current mirror relationship between the third transistor Q3 and the fourth transistor Q4 as shown in the equation 6.

In addition, according to Equation 10 and Equation 11 as follows below, when the current I_c1 and the current I_c3 are increased, reference currents I_12, I_q10 of the bias current I_1b, I_1a of the first amplification circuit unit 60 are decreased, thereby decreasing the bias current I_1a. I_1b of the first amplification circuit unit 60.

[Equation 10]

I_12 $\fallingdotseq$ I_ref - I_c1

[Equation 11]

I_q5 $\fallingdotseq$ I_12 - I_c3

Furthermore, when a voltage of the power controlling terminal VCTRL 73 is decreased, a reference current I_ref of the second amplification circuit unit 80 is divided into a collector current I_q10 of the tenth transistor Q10 and a current I_c4 as follows:

[Equation 12]

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$I\_q10 \fallingdotseq I\_ref - I\_c4.$

Therefore, the collector current of the tenth transistor Q10 is decreased proportionally to increment in the current I_c4, and the bias current of the second amplification circuit unit 80 is decreased due to the current mirror relationship between the tenth transistor Q10 and the twelfth transistor Q12. A high-frequency power of the high-frequency power amplifier proportional to decrement in such a bias current is decreased.

The decreased ratio is the same as a proportional constant determined by a ratio of the first resistor R1 and the second resistor R2 and a ratio of a tenth resistor R10 and a seventeenth resistor R17. The bias currents I_1a, I_1b, I_2 of the first amplification unit and the second amplification circuit unit are exponentially decreased depending on the voltage of a power controlling terminal VCTRL 73. Accordingly, a power mW of high-frequency power amplifier proportional to a square of the bias currents I_1a, I_1b, I_2 is decreased.

Furthermore, converting the power mW into the power dBm, an output power of the antenna is controlled by a unit of dB/V proportionally to the voltage of the power controlling terminal VCTRL 73.

On the other hand, procedures of breaking a power in the power breaking circuit unit will be described as follows.

In the power breaking circuit unit, a fifteenth transistor Q15 is a protection diode for playing a role of protecting an inner circuit of the high-frequency power amplifier by absorbing a static electricity supplied to the power breaking terminal VRAMP 72.

When the voltage of the power breaking terminal VRAMP 72 is

decreased into a ground voltage in order to breaking a power of a high-frequency signal output to the antenna, the current I_ref of voltage-controlled current sources SRC1, SRC2 is broken off by means of a twenty-forth resistor R24, a twenty-fifth resistor R25 and a twenty-third resistor R23.

When the current I_ref is cut off, the bias current I_12 of the fifth transistor Q5 and the bias current of the tenth transistor Q10 is cut off. Therefore, the bias currents I_1a, I_1b of the first amplification circuit unit forming a current mirror relationship with the fifth transistor Q5 and the tenth transistor Q10 and the bias current of the twelfth transistor Q12 of the second amplification circuit unit are cut off.

Accordingly, the current I_ref of the voltage-controlled current source SRC1, SRC2 is broken off or not based on the voltage of the power breaking terminal VRAMP 72 which is a voltage between both sides of the resistor R24.

As described above, according to the communication system employing a high-frequency power amplifier having differential inputs of the present invention, it is possible to maintain performance of the communication system with decreasing the number of components and to reduce production cost, because a signal conversion unit used in the conventional communication system employing a power amplifier having a single input and a single output is not used.